2822




**IN THE UNITED STATES PATENT AND TRADEMARK OFFICE**

Applicant: Leonard Forbes

Title: SILICON-GERMANIUM DEVICES FOR CMOS FORMED BY ION IMPLANTATION AND SOLID PHASE EPITAXIAL REGROWTH

Docket No.: 303.229US2
Filed: August 11, 1998
Examiner: Mark V. Prenty
Serial No.: 09/132,157
Due Date: September 7, 2001
Group Art Unit: 2822

Commissioner for Patents
Washington, D.C. 20231

We are transmitting herewith the following attached items (as indicated with an "X"):

X A return postcard.
X An Amendment and Response (4 Pages).

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CERTIFICATE UNDER 37 CFR 1.8: The undersigned hereby certifies that this correspondence is being deposited with the United States Postal Service with sufficient postage as first class mail, in an envelope addressed to: Commissioner for Patents, Washington, D.C. 20231, on this 7 day of September, 2001.

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(GENERAL)

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#26 D. Scott 9-15-01

**AMENDMENT AND RESPONSE UNDER 37 CFR § 1.111**

Commissioner for Patents
Washington, D.C. 20231

## REMARKS

Applicant has carefully reviewed and considered the Office Action mailed on June 7, 2001, and the references cited therewith.

No amendments or cancellations have been made. Claims 11, 13, 14, 24-28, 32, and 38-43 remain pending in this application.

***§102 Rejection of the Claims***

Claims 11, 14, 24, 28, 38, and 40 were rejected under 35 USC § 102(b) as being anticipated by Selvakumar et al. (U.S. Patent No. 5,426,069).

Claims 25, 32, and 41 were rejected under 35 USC § 102(b) as being anticipated by, or in the alternative under 35 USC § 103(a) as being obvious over Selvakumar et al. (U.S. Patent No. 5,426,069).

Selvakumar appears to show a transistor containing a SiGe channel region 8. However, Selvakumar teaches a "small SiGe region surrounded by silicon" (col. 4, ln. 17-20). As noted by the Examiner in col. 2, ln. 25-28 it appears that in the **background section**, while discussing configurations that are not part of the invention in Selvakumar, the text mentions a hypothesis of a mechanism of a SiGe region, the region being "surrounded by silicon on most of the surfaces." This is not, however, the embodiment taught by Selvakumar. Selvakumar in fact teaches away from creating a $Si_{1-x}Ge_x/SiO_2$ gate oxide interface. As explicitly stated in col. 5, ln. 32-42, Selvakumar teaches:

> "The characteristics of the SiGe MOSFET are believed to be due to the less defective or nearly defect free small SiGe regions **surrounded by silicon all around**. This hypothesis is very similar to the recent discoveries of much reduced misfit dislocation density observed in small area growths (terminated by